METHOD AND DEVICE FOR SEQUENTIAL READOUT OF A MEMORY WITH ADDRESS JUMP

Field of the Invention

The present invention relates to serial access and sequential readout type memories, and more particularly, to a method and device for performing an address jump with such memories.

Background of the Invention

A prior art device for sequential readout of a memory will now be described with reference to the block diagram of FIG. 1. A memory 10 comprising memory cells and address circuits for these cells is read sequentially from one address to the next using a counter 12 whose value, which corresponds to the address of the cell being read, is incremented by one unit each time an INC signal occurs.

The start of the count address is given by a shift register 14 which contains, in addition to the start address in portion 16, the code of the instruction in portion 18. The shift register 14 is loaded by a microcontroller 20, external to the memory, at the rate of the clock pulses CK which are applied to the shift register 14 and to an AND logic gate 22.

An overflow detector 24 for the shift register 14 supplies a signal for opening the AND logic gate 22 as soon as successive shifts lead to a start of

the emptying of the register contents. Further to this opening, the clock pulses CK are applied to a divide-by-N divider circuit 26, where N is the number of bits of a word contained in a memory address, e.g., N = 8 or 16 or 24.

The contents of counter 12 are thus incremented by one unit each time the divider has counted N pulses of the clock, and thus selects the next address. The binary digits of a word at the address selected by the counter 12 are read in succession and are stored in an output shift register 28 at the rate of the clock pulses CK. The binary digits are then sent to the microcontroller 20.

The above description shows that the memory 10 is read sequentially line by line with the counter 12 being incremented by the INC signal appearing at every N pulses of the clock. Each clock pulse corresponds to the readout of a digit forming the binary word contained at the address Ad given by the counter 12.

When the readout is to be carried out with a jump to a new address, the microcontroller must send a new message that contains a jump instruction and a new address. It is thus necessary for the microcontroller 20 to send a complete message, which takes time and reduces the average speed of the operations in a program. This problem is enhanced as the program contains many address jumps.

Summary of the Invention

In view of the foregoing background, an object of the present invention is to provide for the sequential readout of a memory in which address jumps are very fast.

This and other objects, advantages and features according to the present invention are provided by sending to the memory not a complete

message but rather a command signal, i.e., without an address, so that the command signal is interpreted by the memory as indicating that the new address is to use the value of the word contained at the following address.

One aspect of the invention is a method of reading sequentially from a memory implementing an incremental address counter, characterized in that an address jump comprises the following steps:

(a) detecting an address jump signal;

(b) incrementing the incremental address counter;

(c) reading the content of the memory at the incremented address;

(d) transferring the content read at the incremented address into the incremental address counter; and

(e) reading the content of the memory at the address contained in the incremental address counter.

Operation (a) can comprise decoding a jump instruction code. The incrementation of the address counter can be by one unit or more.

Another aspect of the invention is a device for reading sequentially from a memory comprising an input register containing an instruction code and a memory address code, an incremental address counter of the memory which receives the address code from the input register, and an output register of the memory which records signals read at the address indicated by the incremental address counter.

The memory further comprises a detection circuit for detecting an address jump instruction and supplying an incrementation signal for incrementing the incremental address counter, and means for transferring the content read at the incremented address into the incremental address counter.

Brief Description of the Drawings

Other characteristics and advantages of the present invention will become more apparent from reading the following description of a specific embodiment, the description being given in conjunction with the appended drawings, in which:

FIG. 1 is a simplified block diagram of a device for the sequential readout of a memory according to the prior art; and

FIG. 2 is a simplified block diagram of a device for the sequential readout of a memory according to the present invention.

Detailed Description of the Preferred Embodiments

The diagram of FIG. 1 corresponds to a prior art device which has been described above. The diagram of FIG. 2 uses the elements of the diagram of FIG. 1 bearing the same references as well as other elements so as to form the device in accordance with the invention. Those elements which are common to both sequential readout devices will not be described again.

The elements that have been added are as follows. A jump instruction decoder circuit 30 whose input terminals are connected to the output terminals of the shift register 14 correspond to the instruction code. The jump instruction decoder circuit 30 supplies on its three output terminals 30_1, 30_2 and 30_3 three time shifted signals corresponding to the decoding of an address jump.

A first signal, referred to as an address increment signal, on terminal 30_1 is applied to one of the two input terminals of an OR logic gate 36 of which the other input terminal is connected to the output terminal of the divider circuit 26. A second signal, referred to as a transfer signal, on terminal 30_2 is applied to an input terminal of an electronic gate 34 whose other input terminals are connected to the

parallel output terminals of the output shift register 28. A third signal, referred to as a multiplexing signal, on terminal 30_3 is applied to a control input terminal of an address multiplexer circuit 32.

The address multiplexer circuit 32 has a control input terminal connected to the output terminal 30_3 of the decoder circuit 30. The address multiplexer circuit 32 directs to the address counter 12 either the address contained in the shift register 14 or an address read in the memory.

The operation of the device according to the invention is as follows. In a sequential readout, the operation is that of the prior art device. In the case of an address jump, the added elements lead to the following operation. The decoding of the instruction by the decoder circuit 30 produces a first increment signal on output terminal 30_1 which, via the logic gate 36, increments the counter 12 by one unit such that the following address (Ad + 1) of the memory is selected.

When the word at the following address is stored in the output shift register, it is transferred to the multiplexer 32 via the electronic gate 34 which is opened by the transfer signal on output terminal 30_2 of the decoder circuit 30. This transferred word, which corresponds to the following address of the program, is recorded in the counter 12 via the multiplexer circuit 32 controlled by a multiplexing signal supplied on the output terminal 30_3 of the decoder circuit 30.

The sequential readout can then start from that new address or there can be another address jump initiated by the decoding of a new address jump instruction. Instead of using an address jump instruction which is decoded as indicated above, which takes up at least the time to transfer digits of the instruction code, the invention can also be implemented by a specific signal supplied by the microcontroller

20. This signal is applied directly to circuits 32, 34 and 36 with the appropriate delays.